

Target : SAME54 @ 120 MHz (different peripheral set than SAMD51)
fixed flash wait state of 5

bit toggle	execution space	Squarewave Frequency (Mhz)	clock cycles	notes
	flash (alignment/unaligned)	20.0000	6	code fits in pre fetch buffer, alignment doesn't matter
	ram aligned	15.0000	8	slower because of flash always being the master
	ram unaligned	10.0000	12	SRAM needs extra cycles for abritration

ring	execution space	Squarewave Frequency (Mhz)	clock cycles	notes
	flash (unaligned)	3.1578	38	expected as instructions cross memory boudaries
	flash(aligned)	3.3333	36	
	flash (cache enabled, unaligned)	4.0000	30	I-cache doesn't incur the same penalty as SRAM
	flash(cache enabled, aligned)	4.4440	27	
	sram (unaligned)	3.3330	36	aligned sram take a 1 cycle advantage over aligned
	sram (aligned)	4.6158	26	I - cache enabled flash execution